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A New Efficient-Silicon Area MDAC Synapse

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Abstract: Using the binary representation $\sum_i D_i 2^i$ in the Multiplier digital to analog converter (MDAC) synapse designs have crucial drawbacks. Silicon area of transistors, constituting the MDAC circuit, increases exponentially according to the number of bits. This latter is generated by geometric progression of common ratio equal to 2. To reduce this exponential increase to a linear growth, a new synapse named Arithmetic MDAC (AMDAC) is designed. It functions with a new representation based on arithmetic progressions. Using the AMS CMOS 0.35μm technology the silicon area is reduced by a factor of 40%.

Key words: MDAC, binary representation, efficient silicon area

INTRODUCTION

Neural network are very suitable to resolve problems where conventional resolution methods fall[1-3]. Synapses are the common bloc in neural network. It functions as multipliers. Their roles are to weight neural inputs by synaptic weights. Several research aims to implement synapses. Some use numeric implementation whereas others use analogue circuit. Each of these method implementations has its own advantages and drawbacks. Numeric multipliers are very suitable for applications that need high accuracy and precision results[4]. Unfortunately it occupies a considerable silicon area. Analogue synapses are efficient-silicon area and are able to operate at high frequency. However synaptic weights are badly saved in their analogue form[5-13]. To combine the advantages of these last implementation methods, a mixed implementation technique provides best performances[14-22].

A mixed synapse named multiplier digital-to-analogue converter (MDAC) is a multiplier bloc that multiplies an analogue reference by a binary coded synaptic weight. This last is converted by a digital to analogue converter (DAC) to an analogue size, multiplied by the analogue reference and the result is routed to the output of the synapse. Current steering MDAC is the aim of this work for its capability to drive considerable charges at the output of synapses.

Several codes are used to represent the digital synaptic weights[14,15,17,20-22]. The most popular are the thermometer code and the weighted binary code. The advantage of the first cited one is its low glitches.

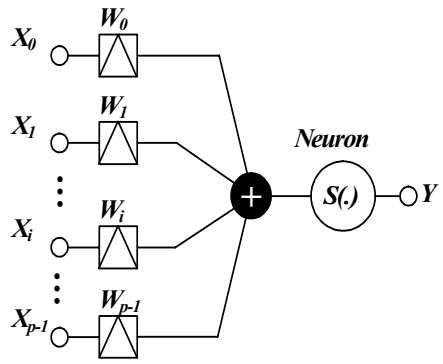

Fig. 1: p-input formal neuron

However to represent N-bits synaptic weight, 2^{N-1} identical current sources are needed. To represent the same weight using binary weighted representation, N current sources, which values follow a geometric progression, are used. The use drawback of such representation is the exponential increase of the current source magnitudes. Face to this problem the design of a new MDAC synapse architecture, called AMDAC, using arithmetic progression will be presented.

Multiplication operation: Neural network are defined as the nonlinear function of weighted sum of signals. The p-inputs of neuron, X_0, X_1… X_{p-1} shown in Fig. 1, are multiplied by the p-synaptic weights, W_0, W_1…, W_{p-1}.

The weighted sum is then forwarded to the neuron output via a nonlinear activation function S(.). Neuron output Y is then given by:

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$$Y = S\left(\sum_{i=0}^{p-1} X_i W_i\right) \quad (1)$$

From the previous equation, multiplication operation of X_iW_i and the addition $\Sigma_iX_iW_i$ are the two arithmetic operation performed by the neuron. The implementation of the addition is easy if outputs of the synapses are currents. It is performed when synapse outputs are connected together according to kirchhoff law (KCL). The difficulty lies in the implementation of the multiplication operation.

The MDAC synapse shown in Fig. 2a is a bloc diagram that multiplies the analog voltage V_{in} by the binary coded synaptic weight $D_{N-1}D_{N-2}\ldots D_2D_1D_0$. The transfer characteristics of MDAC synapse, shown in Fig. 2b and 2c, take two forms. On one hand, when I_{out} current is plotted according to the analog voltage V_{in}, characteristics are straight lines which its slopes vary linearly. On the other hand, I_{out} is a staircase shaped curves when it is plotted according to synaptic weights. From these curves integral nonlinearity error (INL) and differential nonlinearity error (DNL) are concluded. INL is an error characterization between the real staircase shaped curve and the ideal characteristic generally obtained by linear approximation of the real curve.

DNL error give a measure of how well an MDAC can generate uniform smallest analog change LSB. Thus binary synaptic inputs $D_{N-1}D_{N-2}\ldots D_2D_1D_0$ and analog input voltage are combined by the multiplication operation:

$$I_{out} = K \cdot C\left(D_{N-1}, D_{N-2}, \cdots, D_2, D_1, D_0\right) \cdot V_{in} \quad (2)$$

Where I_{out} is the output current of the synapse, K is a constant, V_{in} is the analog input voltage and $C(D_{N-1},D_{N-2},\ldots D_2,D_1,D_0)$ is to binary-to-decimal conversion law. For the weighted binary representation $C(D_{N-1},D_{N-2},\ldots D_2,D_1,D_0)$ is expressed by:

$$C\left(D_{N-1}, D_{N-2}, \cdots, D_2, D_1, D_0\right) = \sum_{i=0}^{N-1} 2^i D_i \quad (3)$$

Binary weighted current steering MDAC

MDAC circuit: The 6-bits MDAC synapse, shown in Fig. 3 is composed of:

* An input circuit converting the analog input voltage V_{in} to a proportional current I_{ref}.
* A series of scaled current mirror so that a mirror produces twice the current produced by the preceding one. Each of the stored bits D_0 to D_6 controls a switch transistor.
* An output circuit inverting the sign of the current I_{sum} issued from current mirrors. The sign circuit determines the direction of the output current, i.e. DI=0 creates a positive (excitatory) synaptic current and DI=1 sets a negative (inhibitory) synaptic current.
* The total output current resulting from the scaled current mirrors is expressed by:

$$I_{sum} = \sum_{i=0}^{5} I_i \frac{V_i}{V_{dd}} \quad (4)$$

Where I_i (i=0…5) is the flowing current in the current mirror i and V_i is the gate voltage controlling the current I_i. V_i takes only either of values V_{dd} or zero. It is then expressed according to the binary value D_i by:

$$V_i = D_i \cdot V_{dd} \quad (5)$$

In the case of D_i=0 then V_i=0. In the other case, when D_i=1 then V_i=V_{dd}. As the size ratio of different current mirrors follow a geometric progression having the common ratio equal to 2, the current I_i is done by:

$$I_i = 2^i I_0 \quad (6)$$

Substituting the equations 5 and 6 in 4 the expression of I_{sum} is done by:

$$I_{sum} = I_0 \cdot \sum_{i=0}^{5} 2^i D_i \quad (7)$$

From the previous equation, the weighted binary to decimal conversion law is shown. Furthermore multiplication operation is shown between the analog input current and the binary to decimal conversion law. Finally, considering the sign bit DI, I_{out} is expressed by:

$$I_{sum} = I_0 \cdot \left(\left(-1^{DI}\right)\sum_{i=0}^{5} 2^i D_i\right) \quad (8)$$

Simulation results of MDAC: Several simulations are carried out using 0.35µm CMOS AMS process. Figure 4 shows good linearity of the V-I converter between input analog voltage V_{in} and the converted current I_{in} from V_{in}=2volt. The linearity of the V-I converter have an impact on the linear variation of the output characteristics. DC analysis show that synaptic output current versus analog input voltage, illustrated in Fig. 5a, follows a linear variation law for each synaptic weight. Linear variation of the slopes is depicted in Fig. 5b. The MDAC output current versus 6-bit synaptic weight is illustrated in Fig. 6. 127 states are represented. INL and DNL normalized to 1 LSB are 3-D represented in Fig. 7. Maximum INL and DNL are respectively equal to 0.7 LSB and 0.6 LSB.

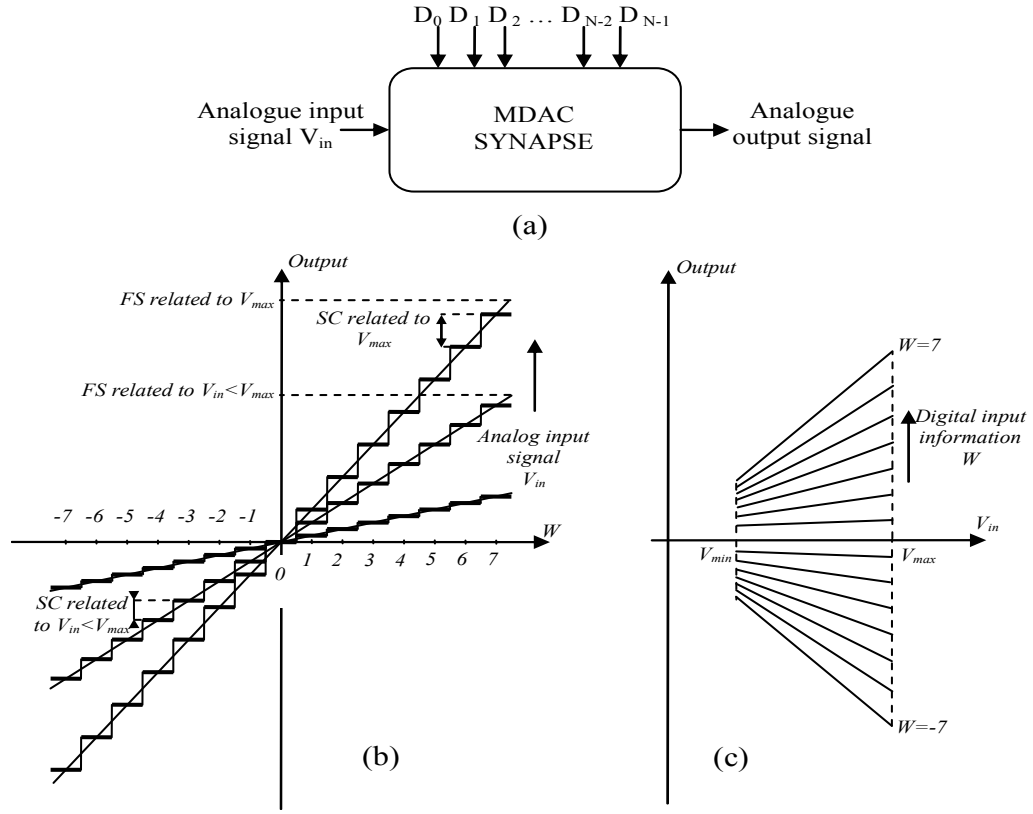


Fig. 2: Simplified schema of a MDAC synapse and its characteristics

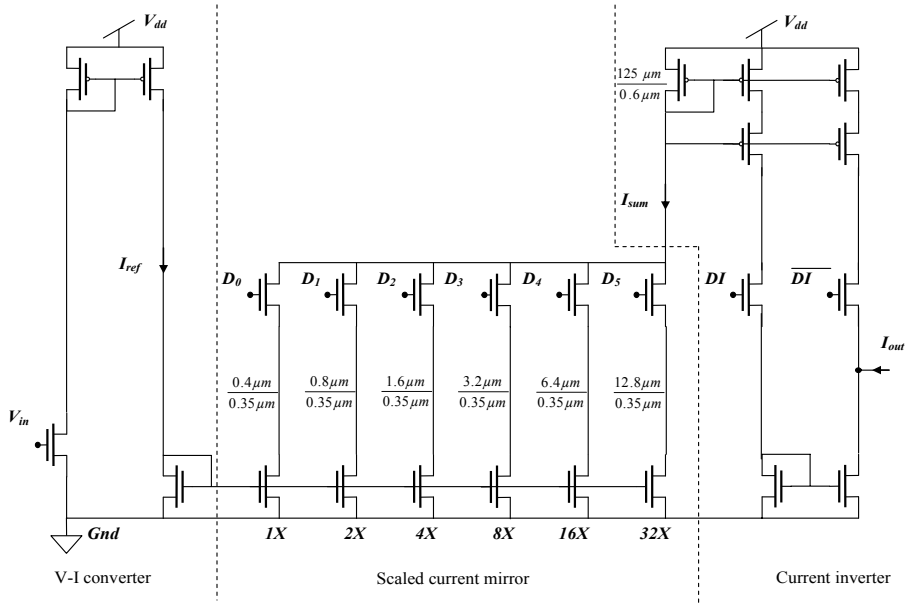


Fig. 3: Weighted binary MDAC circuit

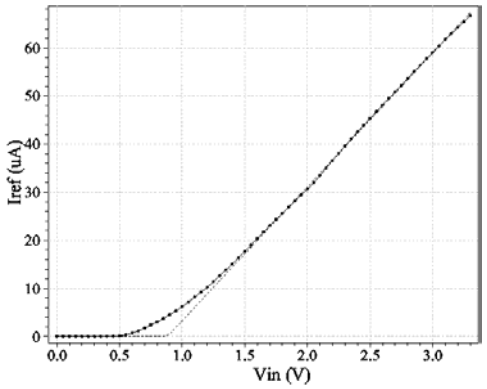
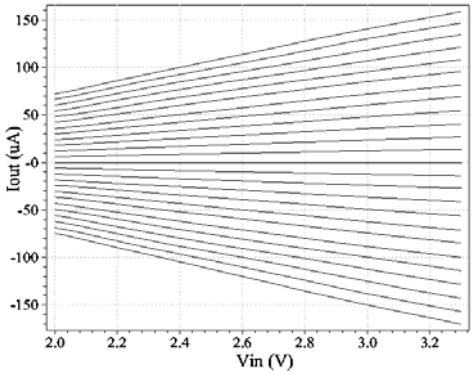
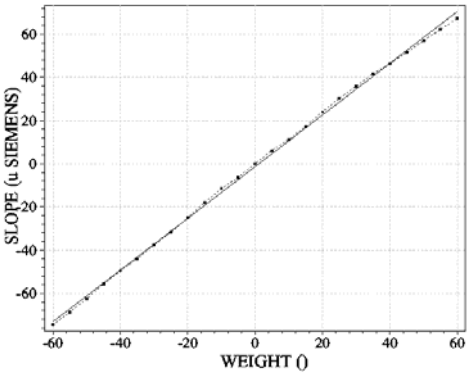


Fig. 4: DC analysis of I_{ref} versus input voltage (solid line) and its linear approximation (dashed line)



(a)



(b)

Fig. 5: (a) DC analysis of MDAC synaptic output current versus input analogue voltage for different synaptic weights (-63…63) (b) Slopes variation of MDAC synaptic output current (dotted curve) and its linear approximation (solid curve)

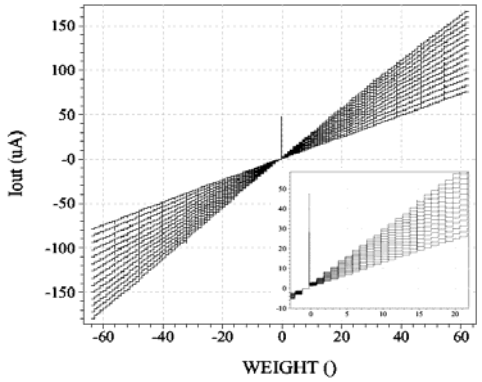


Fig. 6: MDAC Synapse output current versus synaptic weights (±63 level) for various input voltages V_{in} (2.0, 2.1, 2.2… 3.3V)

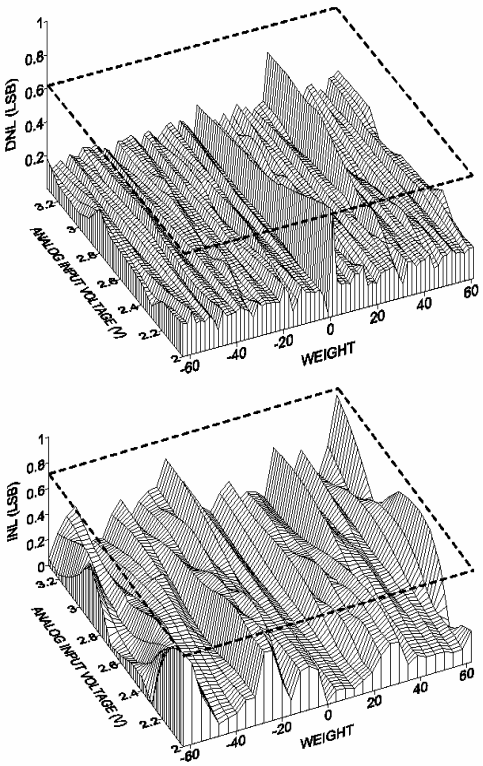


Fig. 7: DNL and INL error of weight binary MDAC

Arithmetic progression based MDAC: AMDAC

From geometric to arithmetic progression:

The MDAC, circuit presented in the previous paragraph, use binary-weighted current mirror widths implanting six current sources of various sizes. Since the current mirror widths are binary weighted, the input code is a simple binary number. The transition from an MDAC state to the following is due to the increase of the total transistor width in conduction by the least significant width (LSW). In the case of our MDAC synapse, LSW is equal to 0.4µm. This last is

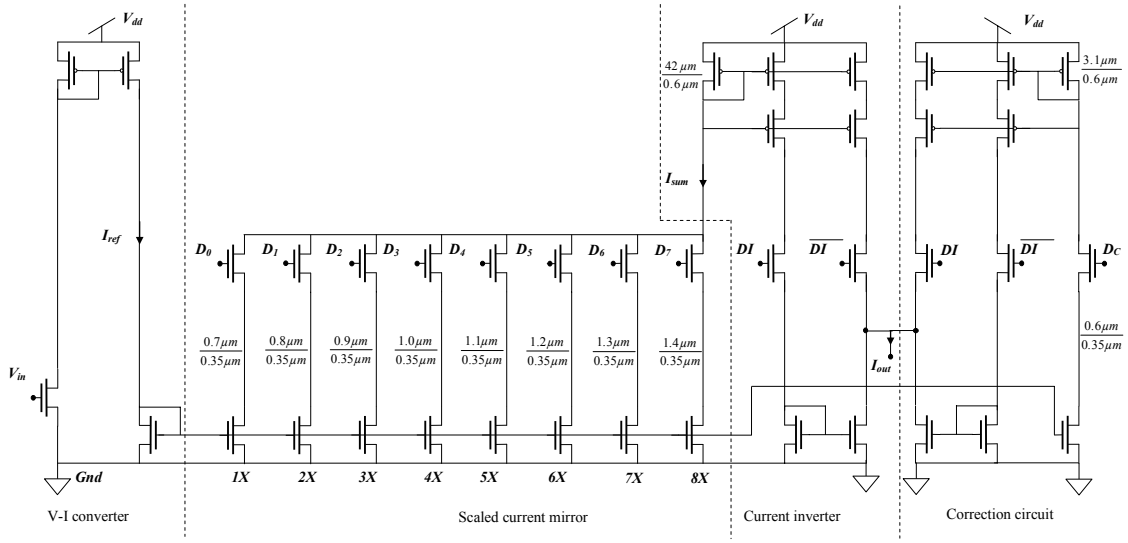


Fig. 8: Circuit of AMDAC synaptic cell

Table 1: 9-bit A2 unsigned binary representation based on arithmetic progression

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	W
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	1	0	0	3
0	0	0	0	1	0	0	0	4
0	0	0	1	0	0	0	0	5
0	0	1	0	0	0	0	0	6
0	1	0	0	0	0	0	0	7
1	0	0	0	0	0	0	0	8
0	0	0	0	0	0	1	1	9
0	0	0	0	0	1	0	1	10
0	0	0	0	1	0	0	1	11
0	0	0	1	0	0	0	1	12
0	0	1	0	0	0	0	1	13
0	1	0	0	0	0	0	1	14
1	0	0	0	0	0	0	1	15
1	0	0	0	0	0	1	0	16
1	0	0	0	0	1	0	0	17
1	0	0	0	1	0	0	0	18
1	0	0	1	0	0	0	0	19
1	0	1	0	0	0	0	0	20
1	1	0	0	0	0	0	0	21
0	1	0	0	0	0	1	1	22
1	0	0	0	0	0	1	1	23
1	0	0	0	0	1	0	1	24
1	0	0	0	1	0	0	1	25
1	0	0	1	0	0	0	1	26
1	0	1	0	0	0	0	1	27
1	1	0	0	0	0	0	1	28
1	1	0	0	0	0	1	0	29
1	1	0	0	0	1	0	0	30
1	1	0	0	1	0	0	0	31
1	1	0	1	0	0	0	0	32
1	1	1	0	0	0	0	0	33
1	0	0	1	0	0	1	1	34
1	0	1	0	0	0	1	1	35
1	1	0	0	0	0	1	1	36
1	1	0	0	0	1	0	1	37
1	1	0	0	1	0	0	1	38
1	1	0	1	0	0	0	1	39
1	1	1	0	0	0	0	1	40
1	1	1	0	0	0	1	0	41
1	1	1	0	0	1	0	0	42
1	1	1	0	1	0	0	0	43
1	1	1	1	0	0	0	0	44
1	1	0	0	0	1	1	1	45
1	1	0	0	1	0	1	1	46
1	1	0	1	0	0	1	1	47
1	1	1	0	0	0	1	1	48
1	1	1	0	0	1	0	1	49
1	1	1	0	1	0	0	1	50
1	1	1	1	0	0	0	1	51
1	1	1	1	0	0	1	0	52
1	1	1	1	0	1	0	0	53
1	1	1	1	1	0	0	0	54
1	1	0	0	1	1	1	1	55
1	1	0	1	0	1	1	1	56
1	1	1	0	0	1	1	1	57
1	1	1	0	1	0	1	1	58
1	1	1	1	0	0	1	1	59
1	1	1	1	0	1	0	1	60
1	1	1	1	1	0	0	1	61
1	1	1	1	1	0	1	0	62
1	1	1	1	1	1	0	0	63
0	1	1	1	1	1	1	1	64
1	0	1	1	1	1	1	1	65
1	1	0	1	1	1	1	1	66
1	1	1	0	1	1	1	1	67
1	1	1	1	0	1	1	1	68
1	1	1	1	1	0	1	1	69
1	1	1	1	1	1	0	1	70
1	1	1	1	1	1	1	0	71

the first term of the geometric progression with which the scaled mirror sizes of the MDAC follow. Consequently, the series of scaled mirror width were:

$$\{0.4\mu m, 0.8\mu m, 1.6\mu m, 3.2\mu m, 6.4\mu m, 12.8\mu m\} \quad (9)$$

The common ratio of the last geometric progression is equal to 2. To handle the transition of a weighted MDAC state to the following, an increase with the two's power of manufacturing grid is enough. Furthermore an arithmetic progression can limit the exponential increase of the geometric progression terms. Its common difference (CD) is equal to two's power of manufacturing grid. Let choose the common difference equal to 0.1µm and the first terms equal to 0.7µm. the eight arithmetic terms are:

$$\left\{\begin{matrix}0.7\mu m, 0.8\mu m, 0.9\mu m, 1.0\mu m,\\ 1.1\mu m, 1.2\mu m, 1.3\mu m, 1.4\mu m\end{matrix}\right\} \quad (10)$$

The Fig. 8 shows the circuit of AMDAC. The V-I converter and the current inverter of the AMDAC are the same that the ones presented in Fig. 3. The scaled mirror sizes follow the arithmetic progression terms of the series-10. Obviously the number representation is not the weighted binary code. A new binary representation based on arithmetic progression named binary arithmetic representation and noted A2 must be established. To represent the first state, 0.7µm-current mirror width is activated. Thus the first number representation is:

$$1\big|_{10} = 00000001\big|_{A2} \quad (11)$$

Where, the $1|_{10}$ and $00000001|_{A2}$ are respectively the notations of the decimal value of one and its A2 binary representation. In this last the only one valued bit is at the least significant bit.

The following states are generated by adding each time the common difference CD equal to 0.1µm. This corresponds to shifting the one valued bit to the more significant bits:

$$\begin{aligned}
2\big|_{10} &= 00000010\big|_{A2}\\
3\big|_{10} &= 00000100\big|_{A2}\\
4\big|_{10} &= 00001000\big|_{A2}\\
5\big|_{10} &= 00010000\big|_{A2}\\
6\big|_{10} &= 00100000\big|_{A2}\\
7\big|_{10} &= 01000000\big|_{A2}\\
8\big|_{10} &= 10000000\big|_{A2}
\end{aligned} \quad (12)$$

The last value, $8|_{10}$, corresponds to the activation of the current mirror having the width equal to 1.4µm. The next value must activate a current mirror width equal to 1.5µm. This last size can be obtained by the activation of the two current mirrors sized W=0.7µm and W=0.8µm. consequently A2 representation of the decimal value $9|_{10}$ is:

$$9\big|_{10} = 00000011\big|_{A2} \quad (13)$$

Higher decimal values are also obtained by shifting one valued bits from the less significant bits towards more significant bits. Table 1 shows the complete eight-bit representation. 71 states are noted. A2 representation is redundant because a decimal value can be represented by several A2 binary codes. For example $00011100|_{A2}$ and $00101010|_{A2}$ activate the same total current mirror width. In fact, the mirrors widths activated by the code $00011100|_{A2}$ are 0.9µm, 1µm and 1.1µm. the total width is then equal to 3µm. the same width can be obtained by the activation of 0.8µm, 1µm and 1.2µm current mirrors. The only forbidden A2 code is 11111111.

Because the first term in the arithmetic series 0.7, 0.8, 0.9…1.4 is not equal to the common difference, a correction bloc must be placed in the circuit represented in Fig. 8 to substrate the equivalent of 0.6µm current mirror width.

The I_{sum} current is expressed by:

$$I_{sum} = \left(\sum_{i=0}^{7} I_i \frac{V_i}{V_{dd}}\right) - I_C \quad (14)$$

Where, I_C is the correction current. For the same length transistor of the scaled mirror, the i^{th} mirrored current I_i is then equal to:

$$I_i = \frac{W_i}{W_0} I_0 = \frac{W_0 + i \cdot CD}{W_0} I_0 \quad (15)$$

Where, W_0 and CD are respectively the common difference and the first term of the arithmetic progression and they are equal to CD=0.1µm and W_0=0.7µm. substituting equation 5, 15 in 14 and considering the sign bit DI the current I_{sum} is expressed by:

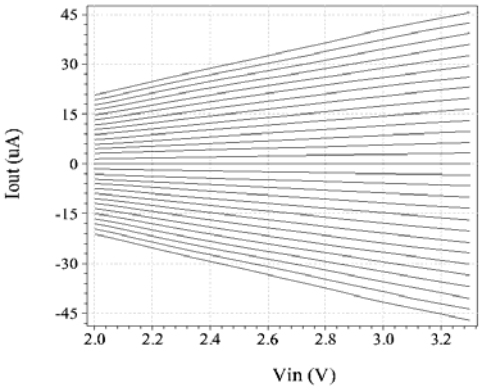
$$I_{sum} = \frac{I_0}{7}\left[(-1)^{DI}\left(7\sum_{i=0}^{7} D_i - 6 + \sum_{i=0}^{7} iD_i\right)\right] \quad (16)$$

The previous equation is a multiplication between the analog current $I_0/7$ and 9-signed-bit A2 representation.

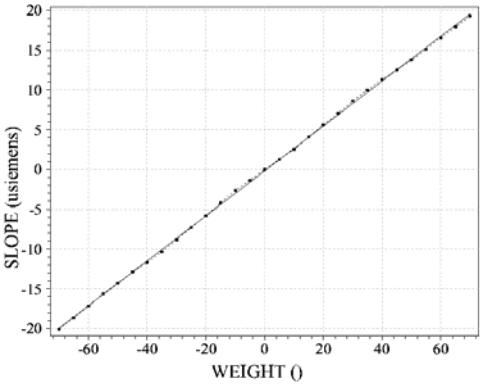
Simulation results of AMDAC: Simulations AMDAC are done in the same conditions as the weighted MDAC simulations. Figure 9a illustrates linear variations of I_{out} versus the analog voltage V_{in}. Figure 9b shows the

Table 2: Performance comparison between 7-signed-bit MDAC and 9-signed-bit AMDAC

Synapse	State number	Maximum full scale	INL error	DNL error	Silicone area
7-signed-bit MDAC	127	166µA	0.7 LSB	0.6 LSB	909 μm^2
9-signed-bit AMDAC	143	70µA	0.7 LSB	0.3 LSB	589μm^2



(a)



(b)

Fig. 9: (a) DC analysis of AMDAC synaptic output current versus input analogue voltage for different synaptic weights (-63…63) (b) Slopes variation of AMDAC synaptic output current (dotted curve) and its linear approximation (solid curve)

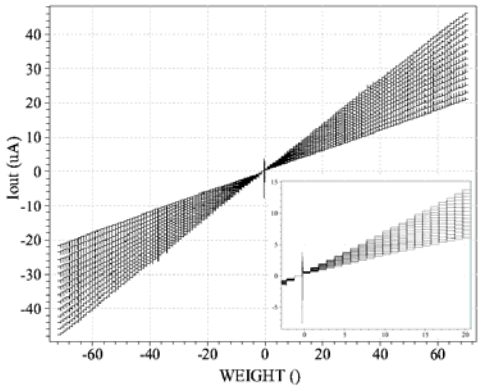


Fig. 10: AMDAC Synapse output current versus synaptic weights (±63 level) for various input voltages Vin (2.0, 2.1, 2.2… 3.3V)

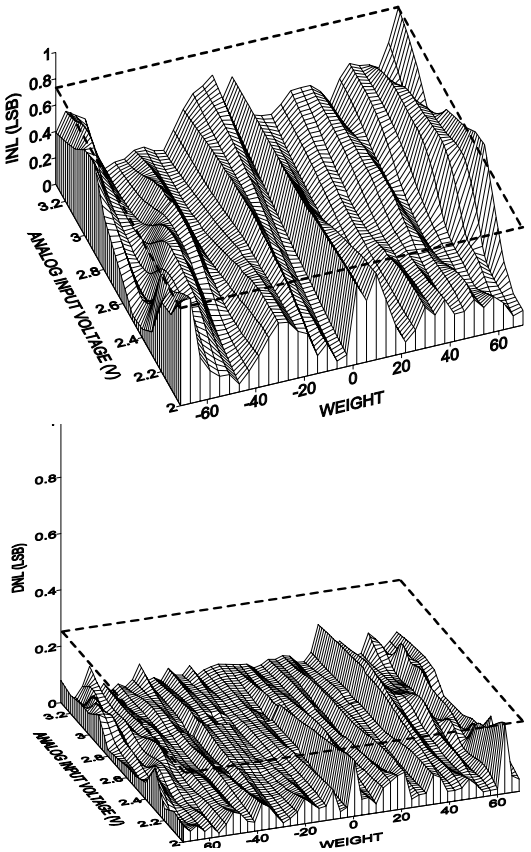


Fig. 11: DNL and INL error of weight binary AMDAC

slope linear variation of the straight line of Fig. 9a. Staircase shaped curves are shown in Fig. 10. From Fig. 11, INL and DNL measures concluded. Maximum INL and DNL error are respectively 0.7 LSB and 0.3 LSB as shown in Fig. 12.

Layout and comparative analysis: Using AMS 0.35µm CMOS process, layouts of 127-state MDAC and 143-state AMDAC are shown in Fig. 12. While the resolution of the latter is higher, its silicon area is lower. Area of AMDAC synapse is 589μm^2 versus MDAC synapse area equal to 909μm^2. Table 2 summarizes the characteristics of the 7-signed-bit MDAC and the 9-signed-bit AMDAC synapses. AMDAC synapse has the lowest silicon area for better precision. For the same INL error, the DNL error of MDAC synapse is higher than AMDAC synapse.

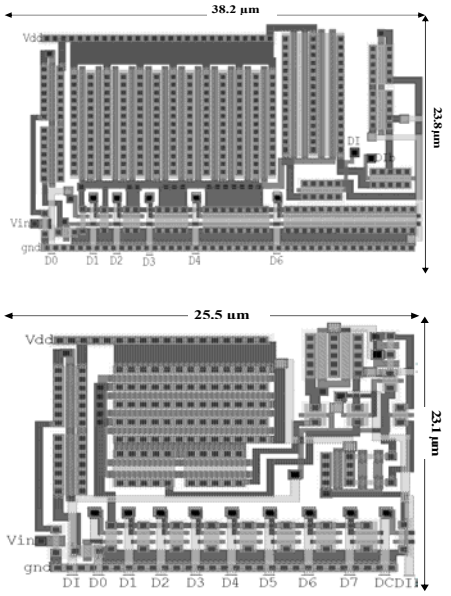


Fig. 12: Layout area of (a) MDAC, (b) A-MDAC

CONCLUSION

In the present work we designed a new multiplier digital-to analog converter based on arithmetic progression called AMDAC. It functions with a new binary representation. We have demonstrated a gain in silicon area by almost of 40% for better resolution compared to classical MDAC.

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