

Comparative Analysis of Reversible Logic Based Carbon Nano Tube Field Effect Transistor Multiplexer Performance

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ABSTRACT

This study is about the design and analysis of a reversible logic based multiplexer, that is realized using carbon nano tube transistor. Reversible logic realization of the digital circuits offers numerous advantages over conventional circuit design. Power analysis was performed using HSPICE simulation software and the results are obtained for the 2×1 and 4×1 multiplexer transient behavior. The power consumption is also obtained. Comparative analysis was performed with the conventional CMOS multipler design to validate the proposed design performance.

Keywords: CNTFET, Demultiplexer, Reversible Logic, Power

1. INTRODUCTION

Recent advancements in the field of Nano science had paved the way for the emerging areas like nano technology, nano electronics. Ever increasing needs of science leads to wide range of advancements in technologies. Nano technology is one such field where ample applications are existing in Bio technology, Bio Medical Science, Medical Science and Research. Shape of the consumer electronics industry has also been changed in the last decade with the evolution of this nano technology. Scaling of the devices has brought the feasible solutions to the burning issues of packaging density and as a result of which a series of new components or devices are emerging, some examples of this category are ultra-scaled FETs, quantum SETs, RTDs, spin devices, superlattice arrays, quantum dots, molecular electronic devices, MODFETs and carbon nanotubes. System level modifications are also taking place with nano electronic components. Low Noise Amplifier designed using high mobility electron transistor is a typical example of the subsystem level advancements at micro and nano level (Sonti and Kannan, 2013).

A typical cross sectional view of CNTFET is as shown in the Fig. 1.

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Fundamental blocks have been designed with various types of nano component models. Gate level modeling results in the design of universal gates at nano level. This creates ripples in the rejuvenation of the art of circuit designing. An example of this development is the design of flip flops, shift registers at this nano level. Principle of CNT device is from the basic laws of electromagnetic, where Lorentz force is responsible for switching between CNT's that are conducting. Features of CNTFET includes lesser cost and high degree of reliability. When gate lengths are scaled down in nanoscales, it results in various crucial challenges and reliability issues that may reduce its potential for energy efficient applications (Murotiya *et al.*, 2012).

Carbon nano tube is embedded between the insulator and the SiO_2 layers. Chirality plays an important role in deciding the electrical characteristics. A carbon Nanotube's band gap is directly affected by its chirality and diameter. If those properties can be controlled, CNTs would be a promising candidate for future nano-scale transistor devices. Typical electrical properties of CNTFETs like higher speed, higher dielectric constant and stability provides good characteristics than Silicon based MOSFETs (Rajendra *et al.*, 2012).

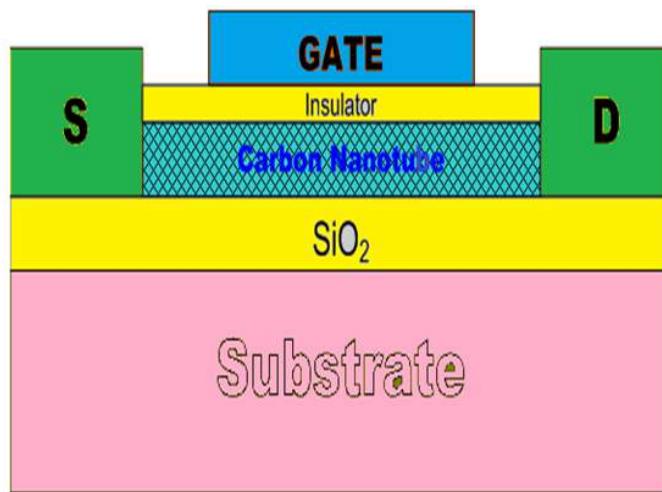


Fig. 1. Ballistic carbon nano tube field effect transistor

Since the I-V characteristics of CNTFETs are quality similar to silicon MOSFET, most of MOS Circuits can be transforming to a CNTFET based design (Ghorbani *et al.*, 2012).

2. TYPES OF CNTFET

The structure of these early devices was very simple. A CNT was positioned so as to bridge two gold or platinum electrodes, which acted as the source and drain of the FET. The exceptional electrical properties of carbon nanotubes arise from the unique electronic structure of graphene itself that can roll up and form a hollow cylinder. There exists different classifications for CNTFET structures. Most common types are 1. Multi Wall CNT (MWCNT) and Single Wall CNT (SWCNT). MWCNT: Each CNT contains several hollow cylinders of carbon atoms nested inside each other and (b) Single-Wall CNT (SWCNT) that is made of just a single layer of carbon atoms. Multi Walled Carbon Nanotubes (MWCNTs) have huge potential for applications in electronics because of both their metallic and semiconducting properties and their ability to carry high current. **Figure 2** represents different types of CNTFET.

The electrical equivalent circuit of a typical CNTFET is as show in the **Fig. 3**.

CNT as a channel in the Field Effect Transistors (FET) of both n-CNFET and p-CNFET types that are used. Because of its very small size, it has been said that a CNT based FET switches reliably using much less power than a silicon based device. Ballistic model of CNTFET has numerous advantages over other models (Rahman *et al.*, 2003; Zhou *et al.*, 2008).

Table 1. The truth table of 2×2 Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Carbon nano tube structures are prominent in reducing the packaging density of the very large scale integrated circuits.

3. REVERSIBLE LOGIC IMPLEMENTATION IN CNTFET

Reversible logic is a method of generation of unique output for every input vector and the converse is true. Equal number of inputs and outputs can be seen in this kind of logic implementation. It is reversible in the sense the gate circuit does not loose the information. Garbage is one which is not used or in other words, every gate output that is not used as the inputs is also known as garbage. **Figure 3** represents reversible logic gate with garbage. **Figure 4** represents typical Feynman gate. **Table 1** represents the truth table of 2×2 Feynman Gate.

Best way to reduce the garbage outputs is to use as many outputs of every gate as possible. Objective can be achieved by using lesser number of reversible gates. Multiplexer is a basic component of many digital circuit design at increased level of complexity. Realization of this multiplexer using the reversible logic and CNTFET is shown in the **Fig. 5 and 6** for the proposed 2×1 and 4×1 multiplexer circuits respectively.

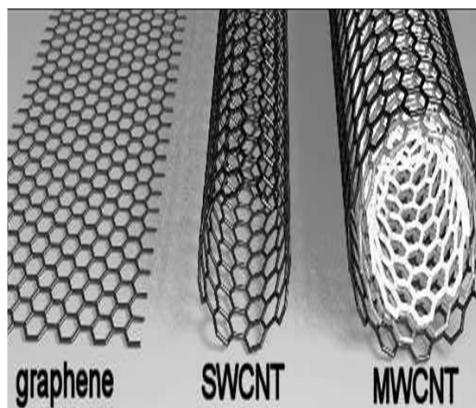


Fig. 2. Types of CNTFET transistors

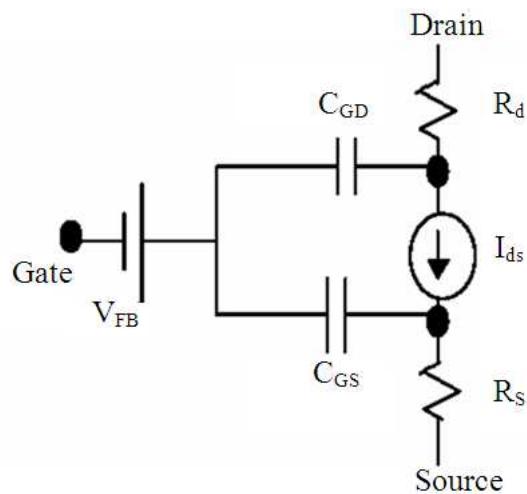


Fig. 3. Electrical equivalent circuit of CNTFET

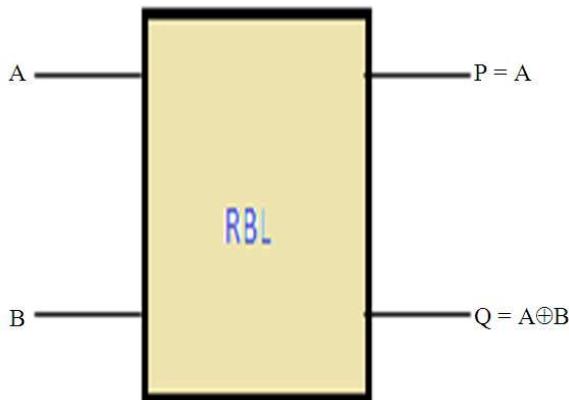


Fig. 4. A typical reversible logic component

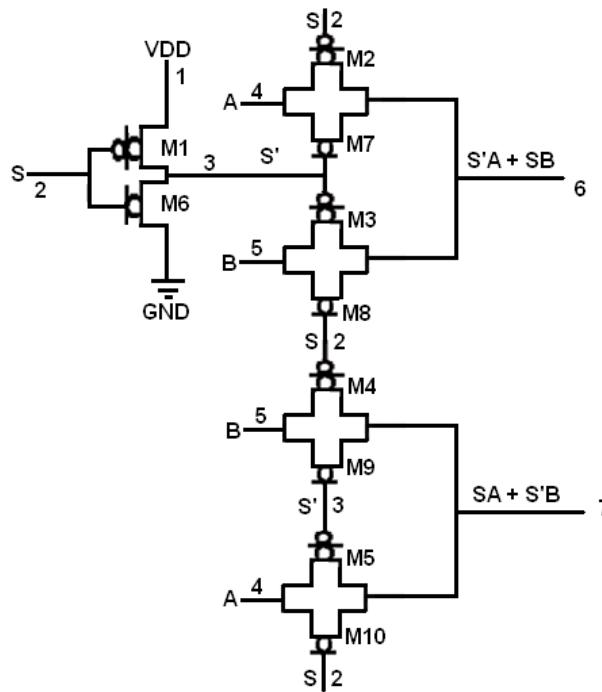


Fig. 5. 2 \times 1 MUX realization

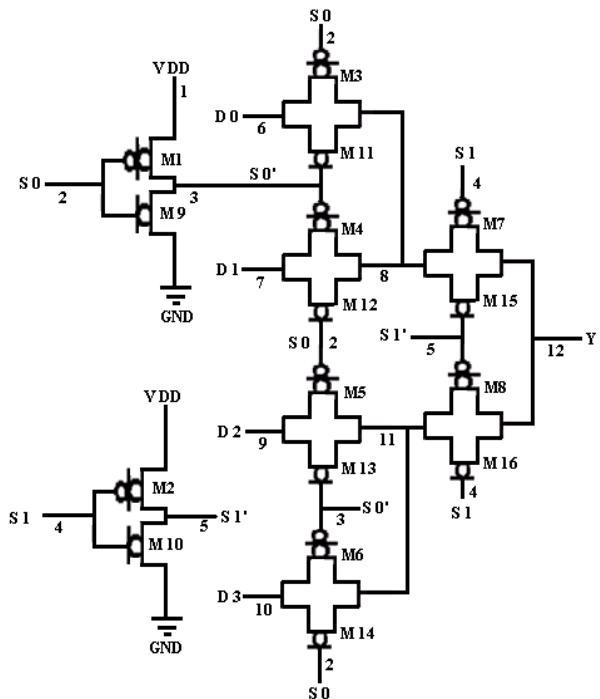


Fig. 6. 4 \times 1 MUX realization



Fig. 7. Transient Response of Reversible Logic 2x1 multiplexer

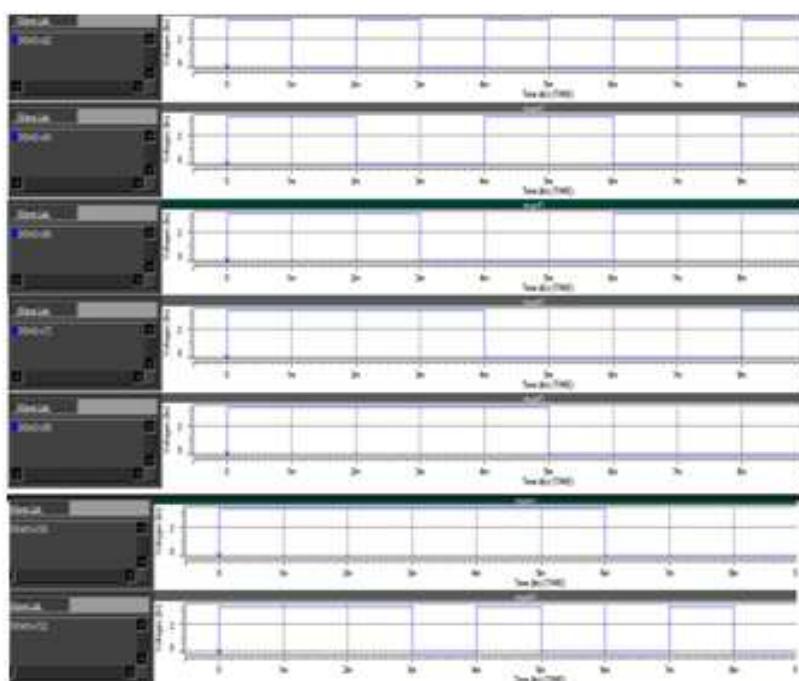


Fig. 8. Transient Response of Reversible Logic 4x1 multiplexer

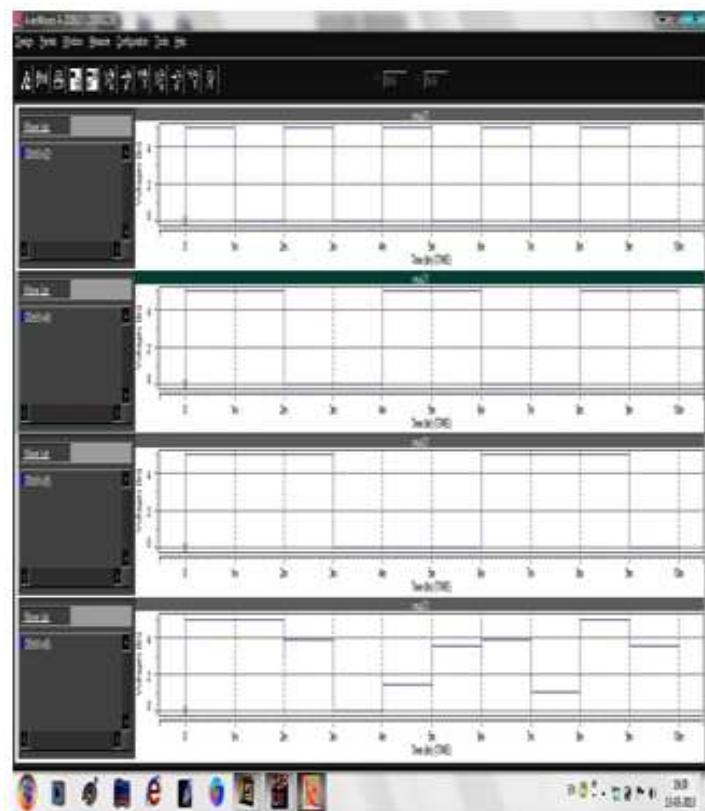


Fig. 9. Transient Response of Reversible Logic based CNTFET 2×1 multiplexer

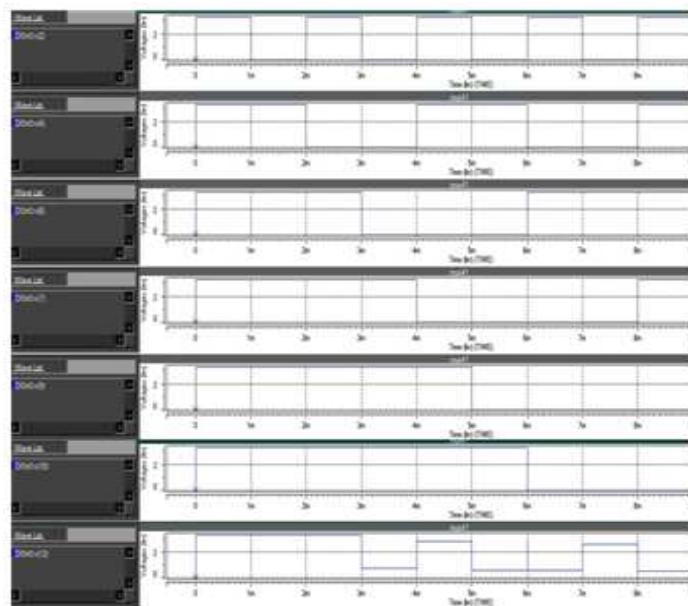


Fig. 10. Transient Response of Reversible Logic based CNTFET 4×1 multiplexer

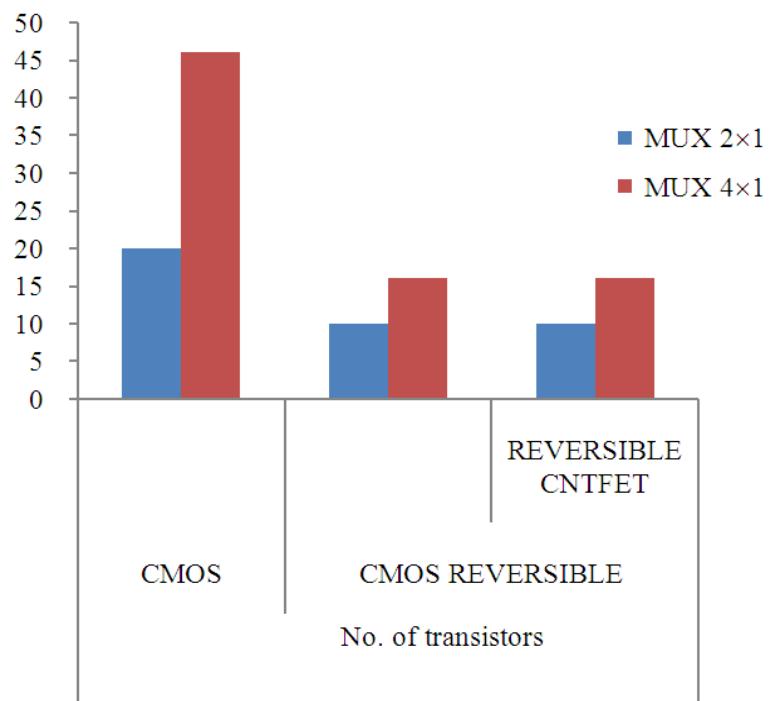


Fig. 11. Number of transistors in different MUX realizations

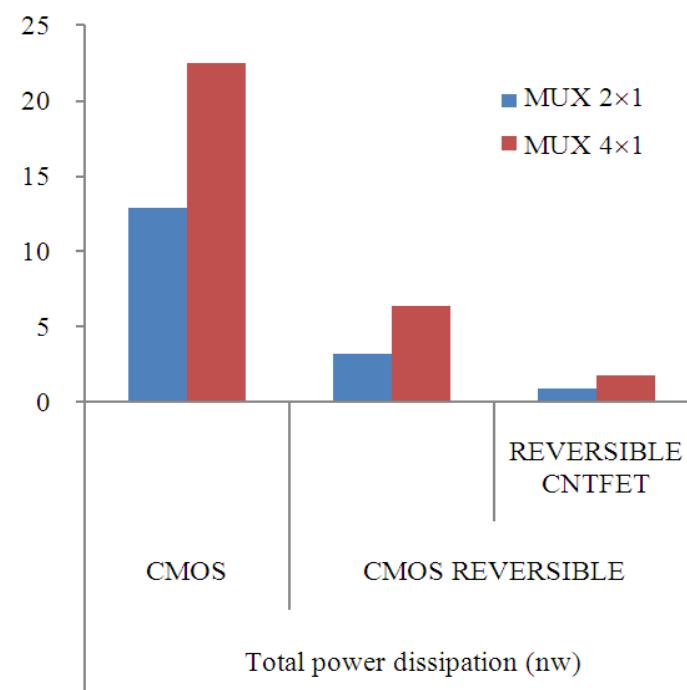


Fig. 12. Number of transistors in different MUX realizations

Table 2. No. of transistors for different multiplexer design

Description	No. of Transistors		
	CMOS	CMOS Reversible	Reversible CNTFET
MUX 2×1	20	10	10
MUX 4×1	46	16	16

Table 3. Power analysis of different multiplexer design

Description	Total power dissipation (nw)		
	CMOS	CMOS Reversible	Reversible CNTFET
MUX 2×1	12.87	3.176	0.86
MUX 4×1	22.53	6.353	1.76

4. RESULTS

Figure 7 and 8 represents the 2×1 and 4×1 demultiplexer transient response using reversible logic respectively.

Figure 9 and 10 represents the 1×2 and 1×4 CNTFET demultiplexer transient response using reversible logic respectively.

Table 2 gives details of number of transistors used in different multiplexer design.

Table 3 elaborates the power consumption of different multiplexer circuits using CNTFET reversible implementation and CMOS implementation.

Figure 11 represents the comparative analysis of number of transistors used in the different types of the multiplexer design. **Figure 12** represents the comparative analysis of the power consumption of the different types of multiplexer circuit design.

5. CONCLUSION

Multiplexer has been designed using CNTFET with reversible logic. Comparison table of power dissipation shows a greatest amount of power reduction has been achieved with the standard CNTFET model over a conventional CMOS. The dynamically reconfigurable universal cells exhibit the possibility to realize dense, regular and highly reconfigurable circuits in platform-based system on chip design. The unwanted growth of metallic tubes during the fabrication of CNTs is a major challenge that will affect the fabrication of robust CNT-based circuits.

6. REFERENCES

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