

A Novel Low-Power CMOS Operational Amplifier with High Slew Rate and High Common-Mode Rejection Ratio

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Abstract: Problem statement: High speed operational amplifier is always an on-going research topic since major high speed application are needed. **Approach:** A two-stage operational amplifier (op amp) is designed, simulated and fabricated using a UMC 0.5 μm 2P2M CMOS technology. **Results:** This chip includes a compensation technique to ensure stability and zero systematic input-offset-voltage. The fabricated chip achieves a 84 dB open loop gain, a 24 $\text{V } \mu\text{S}^{-1}$ slew rate, a 84 dB CMRR utilizing a capacitive load of 5 pF, a 30 MHz unity gain frequency and consumes 2.8 mW from a 2.5 V power supply. **Conclusion:** The proposed chip, which is the first available CMOS operational amplifier in Jordan as the authors are aware, is well-suited to low-voltage applications since it does not require cascade output stages.

Key words: Low-power, CMOS, operational amplifier, slew rate, CMRR

INTRODUCTION

The two-stage circuit architecture has historically been the most popular approach for both bipolar and CMOS op amps, where a complementary process that has reasonable n-type and p-type devices is available (Roberge, 1975). Although this study includes a CMOS version of a two-stage op amp, a bipolar version is similar but slightly more complicated. The two-stage op amp is characterized by its excellent performance when resistive loads need to be driven (Steininger, 1990).

In this study, a two-stage op amp with a high CMRR and a high unity gain frequency is proposed and analyzed. The proposed op amp includes three cascaded stages-two gain stages and a unity-gain output stage necessary for driving resistive loads. The proposed circuit has an open-loop gain of 84 dB, a CMRR of 84 dB, a slew rate of 24 $\text{V } \mu\text{S}^{-1}$, a unity-gain frequency of 30 MHz and consumes 2.8 mW.

MATERIALS AND METHODS

Architecture and circuit implementation: Figure 1 shows the block diagram of the proposed CMOS op amp. It consists of three cascaded stages-two gain stages and a unity-gain output stage necessary for driving resistive loads. The first gain stage is a differential-input single-ended output stage. The second gain stage is a common-

source stage that has an active load. Capacitance C is included to ensure stability when the CMOS op amp is used with feedback. The third stage is a unity-gain stage utilized for driving resistive loads. The complete circuit diagram of this op amp is illustrated in Fig. 2. A brief description of the utilized circuits follows.

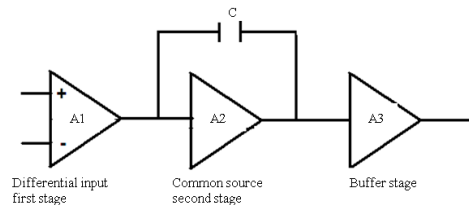


Fig. 1: Block diagram of the two-stage op amp

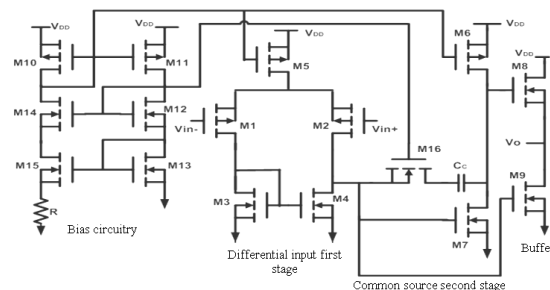


Fig. 2: Circuit diagram of the designed op amp

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Differential-input first stage: The differentially input single ended output stage is formed by the p-channel MOS transistors M1 and M2, loaded in a current mirror formed by the n-channel MOS transistors M3 and M4. Utilizing the p-channel MOS input transistors for this stage is always the best choice to maximize the slew rate since p-channel MOS transistors have low mobility factors. We consider the slew rate an important feature of op amp design. Our choice of p-channel transistors in the first stage will also minimize the flicker noise. The gain of this stage can be expressed as:

$$A_{V1} = g_{m1} (r_{ds2} // r_{ds4}) \quad (1)$$

Common-source second stage: The second stage is simply a common-source gain stage with a p-channel active load M6. This stage has an n-channel input drive transistor M7. This arrangement maximizes the transconductance of the drive transistor in this stage and therefore increasing the unity-gain frequency of the op amp. Such parameters are critical when high frequency operation is desired. The gain of this stage is given by:

$$A_{V2} = -g_{m7} (r_{ds6} // r_{ds7}) \quad (2)$$

Output buffer third stage: The stage is a common-drain buffer stage. In this source follower, the source voltage follows the gate voltage of M8. As shown, the body substrate of M8 is at the same voltage as the source of M8 to eliminate the gain degradations due to the body effect. This connection also results in a smaller dc voltage drop from the gate to the source of M8, which is considered as a major limitation on the maximum positive output voltage. The gain of the source-follower stage is given by:

$$A_{V3} = \frac{g_{m8}}{G_L + g_{m8} + g_{ds8} + g_{ds9}} \quad (3)$$

Biasing circuitry: It is well known that transistor transconductance is an important parameter in op amps that must be stabilized. This stabilization can be achieved by the bias circuitry shown in Fig. 2. In this circuit, the transistor transconductances are matched to the conductance of a resistor. As a result, the transistor conductances are independent of power supply voltage as well as the process and temperature variations.

For the bias circuitry shown in Fig. 2, it is assumed that $(W/L)_{10} = (W/L)_{11}$. This results in, both sides of the circuit, have the same current due to the current-mirror pair M₁₀, M₁₁. As a result, I_{D15} and I_{D13} are equal. Since $V_{GS13} = V_{GS15} + I_{D15} \cdot R_B$, then it can be shown that:

$$g_{m13} = \frac{2 \left(1 - \sqrt{(W/L)_{13} / (W/L)_{15}} \right)}{R_B} \quad (4)$$

Table1: Operational amplifier circuit parameters (L = 1.5 μm)

Component	Value
M ₅ , M ₆ , M ₇	Width = 300 μm
M ₁₀ , M ₁₁ , M ₁₂ , M ₁₃ , M ₁₄	Width = 25 μm
M ₁₅	Width = 100 μm
M ₁ , M ₂	Width = 250 μm
M ₃ , M ₄	Width = 150 μm
M ₁₆	Width = 70 μm
R _b	4 KΩ
C _c	5 pF

Thus, the transconductance of M13 is determined by geometric ratios only and it is independent of power supply and temperature variations. In this design:

$$\left(\frac{W}{L} \right)_{10} = \left(\frac{W}{L} \right)_{11} = \left(\frac{W}{L} \right)_{12} = \left(\frac{W}{L} \right)_{13} = \left(\frac{W}{L} \right)_{14} = \frac{25}{1.5}$$

and for the case:

$$\left(\frac{W}{L} \right)_{15} = 4 \left(\frac{W}{L} \right)_{13}$$

Yields $g_{m13} = 1/R_B$.

As a result, not only g_{m13} is stabilized, but the transconductance of all the other transistors are also stabilized since all transistor currents are derived from the same biasing network and therefore, the ratios of the currents are mainly dependent on geometry.

Compensation circuitry: This circuit is composed of the capacitor C_C which controls the dominant first pole and transistor M₁₆ which operates as a resistor in the triode region. For this circuit it can be shown that (Roberge, 1975) the compensation can be made independent of process and temperature by simply choosing $r_{ds16} = 2/g_{m7}$.

Table 1 shows the physical sizes of all the utilized MOS transistors, resistors and capacitors.

RESULTS

The proposed op amp chip was designed, simulated and fabricated using UMC 0.5 μm 2P2M CMOS technology. The area of the chip is about 220×120 μm. Figure 3 shows the photo the chip.

The measured variation of both the differential gain and the common-mode gain with frequency at 25°C is shown in Fig. 4. From the graph it can be seen that the open-loop gain is 84.3 dB, while the unity gain frequency is 30.5 MHz and the Common-Mode Rejection Ratio (CMRR) is 84.6 dB. This measurement shows that this chip has a high immunity for input noise.

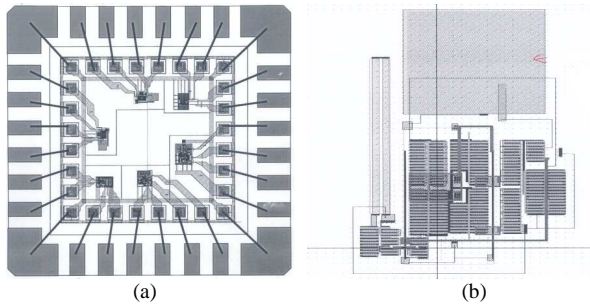


Fig. 3: Photo of the chip. (a) die micrograph of the chip (b) layout of the chip

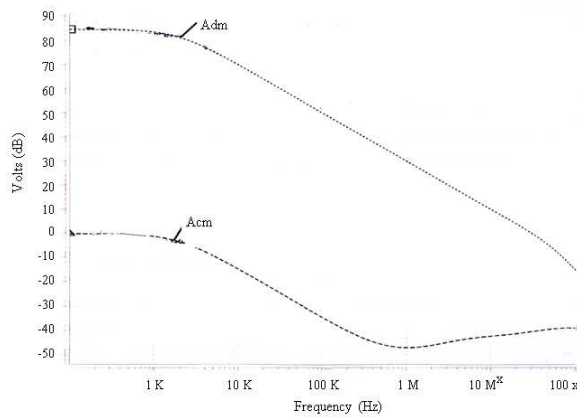


Fig. 4: Variation of the differential and common mode gain

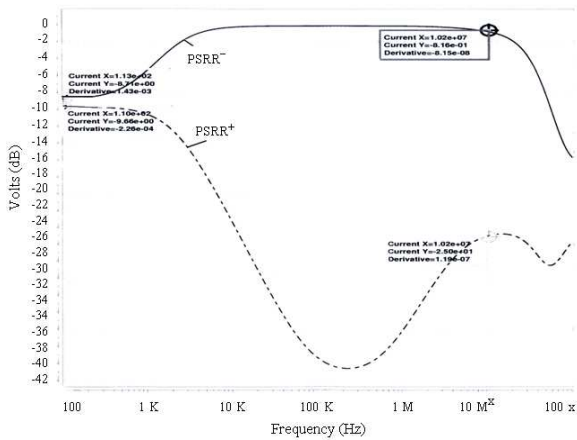


Fig. 5: Measurements of the power supply rejection ratio

The measured variation of the power supply rejection ratio (PSRR) at two different frequencies, namely 100 Hz and 10 MHz is shown in Fig. 5. The Figure 5 shows that the $PSRR^+$ increases from 97.9 dB at 100 Hz to 107 dB at 10 MHz, while $PSRR^-$ decreases from 96.5 dB at 100 Hz to 85.5 dB at 10 MHz.

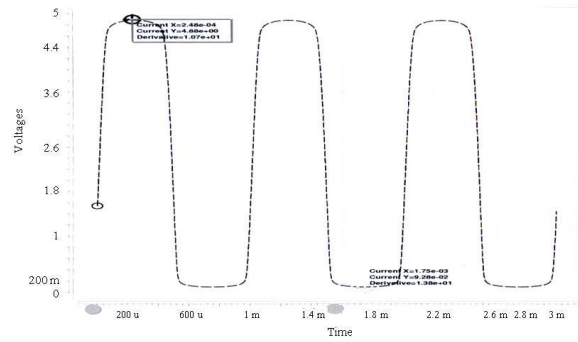


Fig. 6: Measurement of the maximum output voltage swing

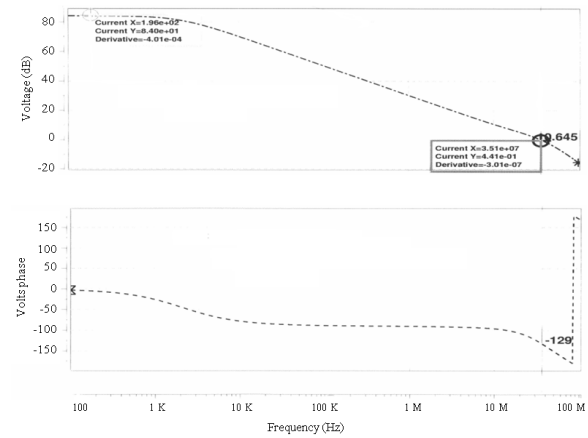


Fig. 7: Bode plot for the fabricated chip

Table 2: Measures op amp performance at different temperatures

Parameter	Measurement @ 25°C	Measurement result at 45°C
Open-loop gain	84.3 dB	84 dB
Unity gain frequency (MHz)	30.5	28.9
Slew rate ($V \mu S^{-1}$)	24.0	24.5
CMRR	84.6 dB	84.5 dB
Phase margin	60°	57°
Power dissipation	2.8 mW	2.8 mW
Offset voltage	7 mV	7 mV
Output voltage swing (Max, Min)	(0.08 and 4.89 V)	Minimum = 0.075 V Maximum = 4.85 V
PSRR 100 Hz	$PSRR^+ = 97.9$ dB	$PSRR^+ = 97.7$ dB
PSRR 10 MHz	$PSRR^- = 96.5$ dB	$PSRR^- = 96.2$ dB
Settling time	0.16 μS	0.18 μS

The variation of the output voltage swing is shown in Fig. 6. The curve shows that the minimum output voltage is 0.08 V and the maximum is 4.89 V which is very close to the supply voltages.

The measured Bode plot for this chip is shown in Fig. 7. From the graph it is clear that the phase margin is 60° while the gain margin is about 15 dB.

In Table 2, the measurement results for the fabricated chip are summarized and compared at both 25 and 45°C temperatures.

DISCUSSION

Utilizing P-channel MOS transistors at the input of the differential input stage increases the slew rate (by decreasing g_m) and provides good immunity against 1/f flicker noise. The utilization of the lead compensation circuit configuration (C_C and transistor M_{16}) is necessary to make compensation independent of the temperature and process variations.

The dc offset voltage is reduced by simply changing the width of transistor M6 (Wu and Nabhan, 2004), taking into consideration that this can also be done by changing the widths of transistors M7, M5 and M4.

Since the utilized biasing circuitry is constant g_m , then a starting circuitry is necessary. Such circuit can be simply built from an externally connected capacitor of 5 μF between VDD and ground (Gray and Meyer, 1993; Sedra and Smith, 1991).

An additional test for the circuit was carried out at two different values of R (when $R = \pm 20\%$ of the nominal value which is 4 K Ω). The test results reveal the goodness of the design since only the slew rate was decreased to about 20 $\text{V } \mu\text{S}^{-1}$ when R was increased to 4.8 K Ω .

CONCLUSION

A 2.5 V CMOS op amp has been designed, simulated and fabricated using UMC 0.5 μm 2P2M CMOS technology. The measurement results indicate that the proposed chip has a 84 dB open loop gain, a 24 $\text{V } \mu\text{S}^{-1}$ slew rate, a 84 dB CMRR utilizing a capacitive load of 5 pF, a 30 MHz unity gain frequency and consumes 2.8 mW from a 2.5 V power supply. Also, it is characterized by its high immunity to flicker noise due to the utilization of p-channel MOS transistors at the input differential stage. Moreover the utilized compensation is independent of temperature and process variations. As far as the authors are aware, this chip is the first available one in Jordan.

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